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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,037	07/11/2003	Jonathan B. Ballagh	X-1208 US	4137

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EXAMINER	
BOWERS, BRANDON	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,037	BALLAGH ET AL.	
	Examiner	Art Unit	
	Brandon W. Bowers	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 18 is objected to because of the following informalities: The use of the word "for" in describing what actions the different sections perform renders the claim indefinite. It is unclear if the action is performed or not by the section. Changing to "an input section that provides" for example will overcome this objection. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Filseth, US Patent No. 5,473,546.

In reference to claims 1, 6, 11, 13, 15, 18, and 21-23, Filseth teaches a method/apparatus/system that performs the steps of identifying an implicit circuit description representing behavior of a first portion of circuit elements within an electronic design (column 7, line 65 – column 8, line 7), augmenting explicit circuit descriptions representing behavior of a second portion of circuit elements within the electronic design with addition circuit information (column 8, lines 8-61), and translating

the electronic design into a circuit description language representation (column 9, line 14 – column 10, line 17).

In reference to claims 7, 12, 14, 16, and 19, Filseth teaches identifying a connection among the implicit circuit description and at least one of the explicit circuit descriptions, adding ports to the implicit circuit description and the at least one of the explicit circuit descriptions responsive to the connection and associating an identifier with the ports added (column 8, lines 8-61).

In reference to claims 3, 8, 17, and 20, Filseth teaches locating two ports to be connected within the electronic design database based on the identifier (column 8, lines 8-61), and adding constructs to the circuit description language representation to effect the connection among the two ports (column 9, line 14 – column 10, line 17).

In reference to claims 4, 5, and 9, Filseth teaches wherein the explicit circuit descriptions and the implicit circuit description are organized over levels of hierarchy within the electronic design and wherein the connections span a plurality of the levels of hierarchy (column 7, line 28 – column 8, line 7).

In reference to claims 2 and 10, Filseth teaches performing the steps of identifying and augmenting for the entire circuit (column 9, line 14 – column 10, line 17).

Claims 1-3, 6-8, and 10-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Wikle et al., US Patent No. 6,684,381.

In reference to claims 1, 6, 11, 13, 15, 18, and 21-23, Wikle teaches a method/apparatus/system that performs the steps of identifying an implicit circuit

description representing behavior of a first portion of circuit elements within an electronic design (column 4, lines 30-52), augmenting explicit circuit descriptions representing behavior of a second portion of circuit elements within the electronic design with addition circuit information (column 5, lines 1-39), and translating the electronic design into a circuit description language representation (column 6, line 66 – column 7, line 55).

In reference to claims 7, 12, 14, 16, and 19, Wikle teaches identifying a connection among the implicit circuit description and at least one of the explicit circuit descriptions, adding ports to the implicit circuit description and the at least one of the explicit circuit descriptions responsive to the connection and associating an identifier with the ports added (column 5, lines 1-39).

In reference to claims 3, 8, 17, and 20, Wikle teaches locating two ports to be connected within the electronic design database based on the identifier, and adding constructs to the circuit description language representation to effect the connection among the two ports (column 5, lines 1-39).

In reference to claims 2 and 10, Wikle teaches performing the steps of identifying and augmenting for the entire circuit (column 4, line 44-52).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

> applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Bening, US Patent No. 6,684,381.

In reference to claims 1, 6, 11, 13, 15, 18, and 21-23, Bening teaches a method/apparatus/system that performs the steps of identifying an implicit circuit description representing behavior of a first portion of circuit elements within an electronic design, augmenting explicit circuit descriptions representing behavior of a second portion of circuit elements within the electronic design with addition circuit information, and translating the electronic design into a circuit description language representation (Column 10, line 40 – column 12, line 63).

In reference to claims 7, 12, 14, 16, and 19, Bening teaches identifying a connection among the implicit circuit description and at least one of the explicit circuit descriptions, adding ports to the implicit circuit description and the at least one of the explicit circuit descriptions responsive to the connection and associating an identifier with the ports added (Column 10, line 40 – column 12, line 63).

In reference to claims 3, 8, 17, and 20, Bening teaches locating two ports to be connected within the electronic design database based on the identifier, and adding constructs to the circuit description language representation to effect the connection among the two ports (Column 10, line 40 – column 12, line 63).

In reference to claims 4, 5, and 9, Bening teaches wherein the explicit circuit descriptions and the implicit circuit description are organized over levels of hierarchy

within the electronic design and wherein the connections span a plurality of the levels of hierarchy (Column 10, line 40 – column 12, line 63).

In reference to claims 2 and 10, Bening teaches performing the steps of identifying and augmenting for the entire circuit (Column 10, line 40 – column 12, line 63).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brandon W. Bowers whose telephone number is (571)272-1888. The examiner can normally be reached on 8:30 am until 5:00 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BWB

VUTHE SIEK
PRIMARY EXAMINER